REMARKS

Claims 30-123 are pending. Although not amended herein, a clean copy of pending claims 30-123 are attached for the Examiner's convenience.

Comment Regarding Applicant's IDSs

The Applicant thanks the examiner for tending to the various IDSs that applicant has submitted in this case. Applicant notes that certain references on the various Form 1449s returned with the 9/25/03 office action had lines drawn through them, with the comment from the Examiner that he did not have copies of these references. However, these same lined-out references appear on other IDSs, and the Examiner has initialed these references on such other IDSs to signify that such references were in fact received and reviewed by the Examiner. Accordingly, as all of the cited references have been initialed by the Examiner on one Form 1449 or another, it appears to the Applicant that all cited references have been received and considered by the Examiner. If the Examiner does not believe this to be correct, and if the Examiner would like to receive copies of certain references, Applicant would appreciate the Examiner telling the Applicant what copies of which references he would like to receive, and they will gladly be supplied.

Double Patenting Rejection

Many of the claims have been rejected for obviousness-type double patenting over USPs 6,287,978, 6,015,760, and 5,880,036, and 5,286,344. Applicant filed a terminal disclaimer to obviate this basis for rejection in his 6/9/03 response to the 5/7/03 office action, but

unfortunately forgot to sign the terminal disclaimer. Applicant further faxed-filed a signed terminal disclaimer to the Examiner on 8/15/03, but it appears that this fax was not received by the Examiner. In any event, the Applicant here again submits a signed terminal disclaimer, along with a power of attorney, which should be suitable to obviate the double patenting rejection.

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The Applicant submits that claims 30-123 are patentable, and requests that a Notice of Allowance issue. The Examiner is invited to contact the undersigned attorney with any questions or comments regarding this paper. (Please note that the undersigned has changed law firms, as reflected in the power of attorney submitted herewith).

Please also note that the Applicant submits herewith papers to correct inventorship for this application. Applicant would appreciate receiving an updated or corrected filing receipt reflecting the inventorship change.

Respectfully submitted,

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Clean Copy of Pending Claims

30. (original) A method of etching a semiconductor wafer comprising a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the silicon oxide layer in an etchant environment comprising a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms, and wherein the etchant environment provides silicon oxide-to-silicon nitride selectivity.

31. (original; reinstated by the examiner) The method of claim 30, wherein the fluorohydrocarbon is CH_3F.

32. (original; reinstated by the examiner) The method of claim 30, wherein the fluorohydrocarbon contains the same number of hydrogen and fluorine atoms.

33. (original; reinstated by the examiner) The method of claim 32, wherein the fluorohydrocarbon is CH_2F_2.

34. (original; reinstated by the examiner) The method of claim 30, wherein the etchant environment further comprises a fluorinated gas.

35. (original; reinstated by the examiner) The method of claim 34, wherein the fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

36. (original; reinstated by the examiner) The method of claim 34, wherein the etchant environment further comprises an inert gas.

37. (original; reinstated by the examiner) The method of claim 36, wherein the inert gas is argon.

38. (original; reinstated by the examiner) The method of claim 30, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

39. (original; reinstated by the examiner) The method of claim 30, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

40. (original; reinstated by the examiner) The method of claim 30, wherein the silicon nitride layer is formed with an uneven topography.

41. (original; reinstated by the examiner) The method of claim 30, wherein the semiconductor wafer further comprises two polysilicon conductors, wherein the silicon nitride

layer is formed above the polysilicon conductors, and wherein the plasma etching forms an opening in the silicon oxide between the polysilicon conductors.

42. (original) The method of claim 30, further comprising heating the semiconductor wafer during plasma etching.

43. (original; reinstated by the examiner) The method of claim 42, wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

44. (original; reinstated by the examiner) The method of claim 42, wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

45. (original; reinstated by the examiner) The method of claim 42, wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

46. (original; reinstated by the examiner) The method of claim 42, wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

47. (original; reinstated by the examiner) The method of claim 46, wherein the electrode is heated to between about 20 and 80 degrees C.

48. (original; reinstated by the examiner) The method of claim 46, wherein the electrode is heated to between about 30 and 60 degrees C.

49. (original; reinstated by the examiner) The method of claim 46, wherein the electrode is heated to between about 35 and 50 degrees C.

50. (original; reinstated by the examiner) The method of claim 42, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the wafer chuck.

51. (original; reinstated by the examiner) The method of claim 50, wherein the wafer chuck is heated to at least about 30 degrees Celsius.

52. (original; reinstated by the examiner) The method of claim 50, wherein the wafer chuck is heated to from about 30 to about 100 degrees Celsius.

53. (original; reinstated by the examiner) The method of claim 42, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the etch chamber side wall.

54. (original; reinstated by the examiner) The method of claim 53, wherein the side wall is heated to at least about 50 degrees Celsius.

55. (original; reinstated by the examiner) The method of claim 54, wherein the side wall is heated to from about 50 to 100 degrees Celsius.

56. (original) The method of claim 42, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the wafer chuck and heating the etch chamber side wall.

57. (original) The method of claim 56, wherein the wafer chuck is heated to at least about 30 degrees Celsius, and wherein the side wall is heated to at least about 50 degrees Celsius.

58. (original) The method of claim 56, wherein the wafer chuck is heated to from about 30 to about 100 degrees Celsius.

59. (original) The method of claim 56, wherein the side wall is heated to from about 50 to 100 degrees Celsius.

60. (original; reinstated by the examiner) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 10-to-1.

61. (original; reinstated by the examiner) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

62. (original; reinstated by the examiner) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

63. (original) A method of etching a semiconductor wafer comprising a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the semiconductor wafer in an etchant environment, wherein the method comprises heating the semiconductor wafer during plasma etching to increase the silicon oxide-to-silicon nitride selectivity.

64. (original; reinstated by the examiner) The method of claim 63, wherein the etchant environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms.

65. (original; reinstated by the examiner) The method of claim 64, wherein the fluorohydrocarbon is CH_3F.

66. (previously amended; reinstated by the examiner) The method of claim 63, wherein the etchant environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains the same number of hydrogen and fluorine atoms.

67. (original; reinstated by the examiner) The method of claim 66, wherein the fluorohydrocarbon is CH_2F_2.

68. (original; reinstated by the examiner) The method of claim 63, wherein the etchant environment further comprises a fluorinated gas.

69. (original; reinstated by the examiner) The method of claim 68, wherein the fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

70. (original; reinstated by the examiner) The method of claim 68, wherein the etchant environment further contains an inert gas.

71. (original; reinstated by the examiner) The method of claim 70, wherein the inert gas is argon.

72. (original; reinstated by the examiner) The method of claim 63, wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

73. (original; reinstated by the examiner) The method of claim 63, wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

74. (original; reinstated by the examiner) The method of claim 63, wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

75. (original; reinstated by the examiner) The method of claim 63, wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

76. (original; reinstated by the examiner) The method of claim 75, wherein the electrode is heated to between about 20 and 80 degrees C.

77. (original; reinstated by the examiner) The method of claim 75, wherein the electrode is heated to between about 30 and 60 degrees C.

78. (original; reinstated by the examiner) The method of claim 75, wherein the electrode is heated to between about 35 and 50 degrees C.

79. (original; reinstated by the examiner) The method of claim 63, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the wafer chuck.

80. (original; reinstated by the examiner) The method of claim 79, wherein the wafer chuck is heated to at least about 30 degrees Celsius.

81. (original; reinstated by the examiner) The method of claim 79, wherein the wafer chuck is heated to from about 30 to about 100 degrees Celsius.

82. (original; reinstated by the examiner) The method of claim 63, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor

wafer and etch chamber side wall, and wherein heating the semiconductor wafer involves heating the etch chamber side wall.

83. (original; reinstated by the examiner) The method of claim 82, wherein the side wall is heated to at least about 50 degrees Celsius.

84. (original; reinstated by the examiner) The method of claim 82, wherein the side wall is heated to from about 50 to 100 degrees Celsius.

85. (original) The method of claim 63, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the wafer chuck and heating the etch chamber side wall.

86. (original) The method of claim 85, wherein the wafer chuck is heated to at least about 30 degrees Celsius, and wherein the side wall is heated to at least about 50 degrees Celsius.

87. (original) The method of claim 85, wherein the wafer chuck is heated to from about 30 to about 100 degrees Celsius.

88. (original) The method of claim 85, wherein the side wall is heated to from about 50 to 100 degrees Celsius.

89. (original; reinstated by the examiner) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 10-to-1.

90. (original; reinstated by the examiner) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than 20-1.

91. (original; reinstated by the examiner) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

92. (original; reinstated by the examiner) The method of claim 63, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

93. (original; reinstated by the examiner) The method of claim 63, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

94. (original; reinstated by the examiner) The method of claim 63, wherein the silicon nitride layer is formed with an uneven topography.

95. (original; reinstated by the examiner) The method of claim 63, wherein the semiconductor wafer further comprises two polysilicon conductors, wherein the silicon nitride layer is formed above the polysilicon conductors, and wherein the plasma etching forms an opening in the silicon oxide between the polysilicon conductors.

96. (original) A method of etching a semiconductor wafer containing a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the semiconductor wafer using an etch environment that provides a silicon oxide-to-silicon nitride selectivity of greater than or equal to 10-to-1.

97. (original; reinstated by the examiner) The method of claim 96, wherein the etch environment comprises a first gas selected from the group comprising CH_3F and CH_2F_2.

98. (original; reinstated by the examiner) The method of claim 97, wherein the etch environment further comprises a second fluorinated gas.

99. (original; reinstated by the examiner) The method of claim 98, wherein the second fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

100. (original; reinstated by the examiner) The method of claim 98, wherein the etch environment further comprises an inert gas.

101. (original; reinstated by the examiner) The method of claim 100, wherein the inert gas is argon.

102. (original) The method of claim 96, further comprising heating the semiconductor wafer during plasma etching.

103. (original; reinstated by the examiner) The method of claim 102, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the wafer chuck.

104. (original; reinstated by the examiner) The method of claim 103, wherein the wafer chuck is heated to at least about 30 degrees Celsius.

105. (original; reinstated by the examiner) The method of claim 103, wherein the wafer chuck is heated to from about 30 to about 100 degrees Celsius.

106. (original; reinstated by the examiner) The method of claim 102, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the etch chamber side wall.

107. (original; reinstated by the examiner) The method of claim 106, wherein the side wall is heated to at least about 50 degrees Celsius.

108. (original; reinstated by the examiner) The method of claim 106, wherein the side wall is heated to from about 50 to 100 degrees Celsius.

109. (original) The method of claim 102, wherein the method is performed within an etch chamber comprising a wafer chuck for holding the semiconductor wafer and an etch chamber side wall, and wherein heating the semiconductor wafer involves heating the wafer chuck and heating the etch chamber side wall.

110. (original) The method of claim 109, wherein the wafer chuck is heated to at least about 30 degrees Celsius, and wherein the side wall is heated to at least about 50 degrees Celsius.

111. (original) The method of claim 109, wherein the wafer chuck is heated to from about 30 to about 100 degrees Celsius.

112. (original) The method of claim 109, wherein the side wall is heated to from about 50 to 100 degrees Celsius.

113. (original) The method of claim 112, wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 10-to-1 but less than or equal to 33-to-1.

114. (original) The method of claim 113, wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 10-to-1 but less than or equal to 50-to-1.

115. (original; reinstated by the examiner) The method of claim 96, wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

116. (original; reinstated by the examiner) The method of claim 115, wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 20-to-1 but less than or equal to 33-to-1.

117. (original; reinstated by the examiner) The method of claim 116, wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 20-to-1 but less than or equal to 50-to-1.

118. (original; reinstated by the examiner) The method of claim 96, wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

119. (original; reinstated by the examiner) The method of claim 118, wherein the silicon dioxide-to-silicon nitride selectivity is greater than or equal to 30-to-1 but less than or equal to 50-to-1.

120. (original; reinstated by the examiner) The method of claim 96, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

121. (original; reinstated by the examiner) The method of claim 96, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

122. (original; reinstated by the examiner) The method of claim 96, wherein the silicon nitride layer is formed with an uneven topography.

123. (original; reinstated by the examiner) The method of claim 96, wherein the semiconductor wafer further comprises two polysilicon conductors, wherein the silicon nitride layer is formed above the polysilicon conductors, and wherein the plasma etching forms an opening in the silicon oxide between the polysilicon conductors.